Fabrication of Graphene Double Quantum Dot Devices by He-ion Beam Milling

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Abstract

Graphene, a single layer of carbon atoms arranged in a honeycomb pattern, is considered as a wonder material due to its remarkable properties. Small spin-orbit and hyperfine interactions have been theoretically predicted [1,2], which make graphene a promising option for Quantum Information Technologies (QIT) and spin qubit embodiment.

Currently, e-beam lithography (EBL) followed by reactive ion etching (RIE) is the most established method for fabricating graphene devices. However, proximity effects, e-beam spot size, undercutting of resists during etching and uneven distribution of resist layer (thickness-wise), which may be caused by the presence of graphite pieces, metallic alignment marks, and roughness of the SiO_2 substrate on the sample surface, can limit the resolution of devices fabricated by this method. Helium-ion microscopy (HIM) is a new surface imaging technique that involves scanning a focused beam of helium ions across a sample surface and generating an image from the emitted secondary electrons (SE). An atomically sharp and extremely bright source, combined with the larger momentum (and so smaller de Broglie wavelength) of helium ions compared to electrons, enables a sub-nanometer probe size at the sample surface and high resolution imaging, below 0.35 nm in some systems [3-5].

In this work, we demonstrate a novel fabrication method by combining the EBL and HIM milling to fabricate high resolution GDQDs devices. Helium ion milling is then used to pattern the flakes with intricate DQDs devices, with sub 10 nm resolution and high fidelity. This hybrid fabrication approach could pave the way to a better understanding and more detailed study of graphene quantum devices. Figure 1 compares one of our GDQDs devices fabricated by standard e-beam lithography and RIE etch (Figure 1a) and a high resolution DQDs pattern milled on a monolayer flake by HIM milling (Figure 1b).
Graphene flakes were produced by mechanical exfoliation and were transferred onto highly doped Si substrates with a 295 nm-thick SiO_2 top layer. EBL, metallization and lift-off processes were employed to fabricate metal contacts onto the deposited flakes. To minimize e-beam induced defects in the graphene flakes, a ~ 460 nm-thick layer of *Methyl Methacryllate* (MMA) 8.5 resist was used. The soft nature of MMA resist allows the use of a low e-beam base dose (110 $\mu C/cm^2$), at an acceleration voltage of 100 kV. Metallization of the samples was carried out by evaporation of Ti/Au (5 nm/55 nm), followed by lift-off. EBL and RIE was then employed to introduce isolation lines on the flakes, separating the metal contacts and leaving an area of approximately 500 nm × 500 nm for the final HIM milling step (Figure 1c). For the second lithography step (to define the isolation lines), a ~40 nm-thick layer of PMMA 495K resist was exposed by a constant e-beam dose of 190 $\mu C/cm^2$. The exposed patterns were then transferred onto the flakes by RIE etch in Ar/O_2 (4:1) gas flow with RF power of 35 W. HIM milling was carried out using a OrionPlus^{TM} helium ion microscope (Carl Zeiss) operated with a beam current of 1 pA at an accelerating voltage of 30 kV. Initial dose tests on pristine graphene showed a He-dose of 0.63 $nC/\mu m^2$ is adequate to mill desired patterns on a monolayer graphene. However, milling using the same dose was not successful when applied to e-beam processed samples. The milled patterns were not so clearly defined compared to those produced on pristine flakes and there was evidence of accumulation rather than removal of material in the scanned area. This was due to residues remaining on the surface following the exposure of graphene to resists and solvents during e-beam processing [6]. An annealing process was therefore developed whereby e-beam processed samples were annealed at ~320°C in 1.3 L/min forming gas flow (6% H_2 and 94% N_2) after 2 h in an atmospheric furnace. This step reduces surface contaminants sufficient to allow successful HIM milling of DQDs patterns (Figure 2a), using a dose of 0.63 $nC/\mu m^2$.

Results from room temperature measurements of the forward (I_{SD}) and the reverse (I_{DS}) source-drain current through a device with the same dimensions as the device shown in Figure 2a, as a function of the applied source-drain voltage (V_{SD}) are presented in Figure 2b. For a bias voltage of 5 mV the current through the device was 130 pA with almost no current leakage from the channel and the DQDs. To confirm complete milling of the graphene exposed to the He beam and therefore successful isolation of all side gates, the device was measured for possible gate leakage between the side-gates and the channel. The currents measured between all side gates lie within the noise levels of the measurement equipment (in fA range, Figure 2c) and so can be considered to be negligible, indicating successful isolation of all side gates. This proved that accurate alignment between the e-beam pattern and the HIM pattern was achieved and the developed milling conditions were adequate to completely mill the flake with the desired pattern with a high yield. This work demonstrates that HIM milling has the potential to enable fine-scale fabrication of nanoelectronic devices in graphene and could ultimately pave the way towards observation of Coulomb blockade at room temperature in GQDs devices.

References

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Figures

(a) **(b)** **(c)**

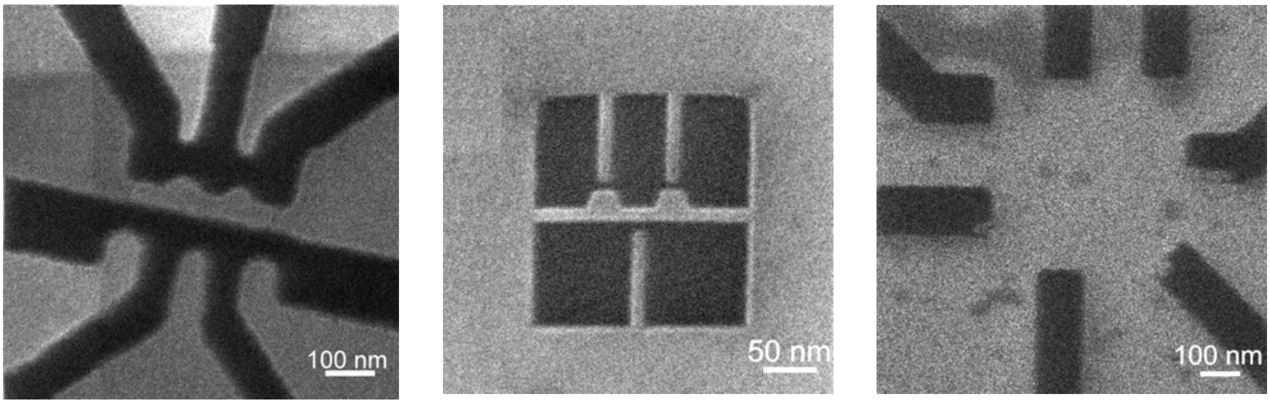

Figure 1. HIM SE imaging: (a) A GDQDs device fabricated by standard e-beam lithography and RIE etch; (b) A high resolution DQDs pattern milled on a monolayer flake by HIM milling. The distances between the side-gates and the QDs are less than 8 nm; (c) The isolation lines fabricated by EBL and RIE on monolayer graphene flake.

(a) **(b)** **(c)**

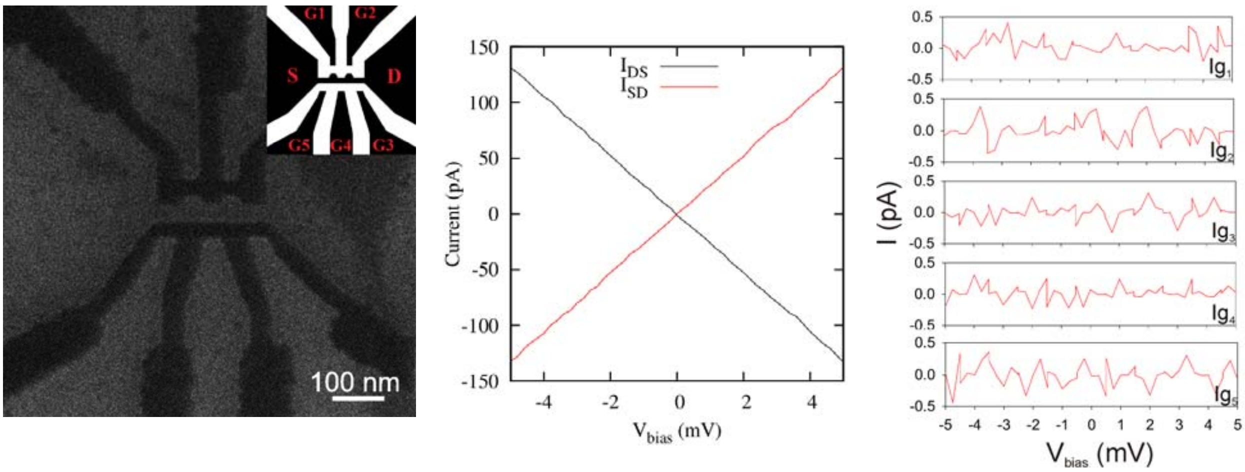

Figure 2. (a) A DQD device milled into a metal-contacted graphene flake using a helium ion dose of 0.63 nC/μm^2, with the design of HIM milling pattern to define DQD device (upper right inset); (b) I-V measurement results for source-drain channel; (c) Gate leakage I-V measurement results.